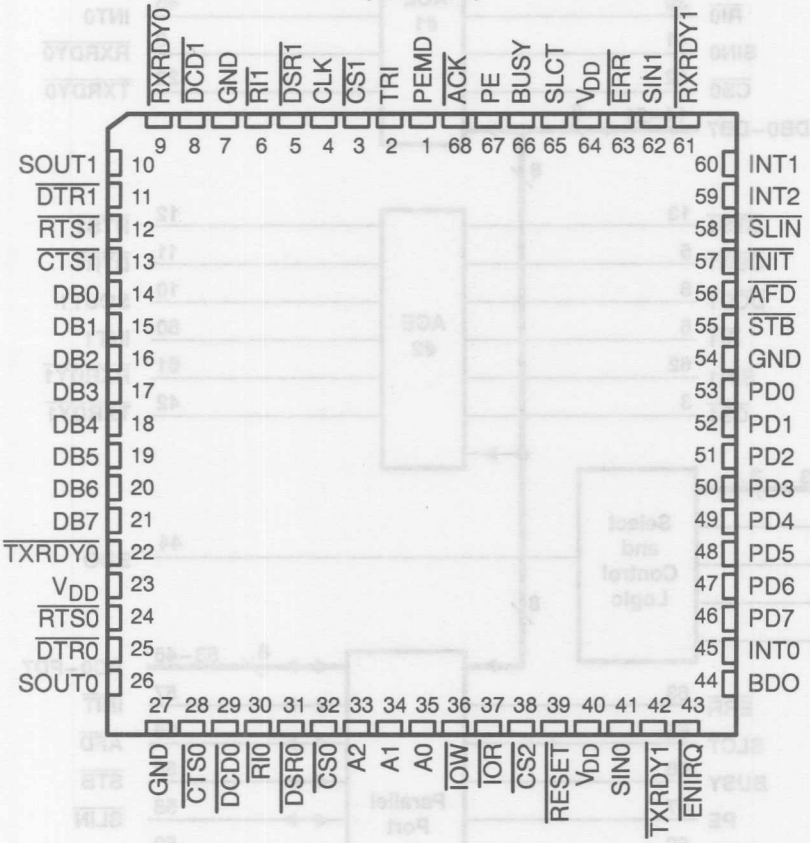
- IBM PC/AT Compatible
- Two TL16C550 ACEs
- Enhanced Bidirectional Line-Printer Port
- 16-Byte FIFOs Reduce CPU Interrupts
- Up to 16-MHz Clock Rate for up to 1-Mbaud Operation
- Independent Control of Transmit, Receive, Line Status, and Data-Set Interrupts on Each Channel
- Individual Modem-Control Signals for Each Channel
- Programmable Serial-Interface Characteristics for Each Channel:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity-Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop-Bit Generation
- 3-State Outputs Provide TTL Drive for the Data and Control Bus on Each Channel
- Hardware and Software Compatible With TL16C452

FN PACKAGE
(TOP VIEW)



description

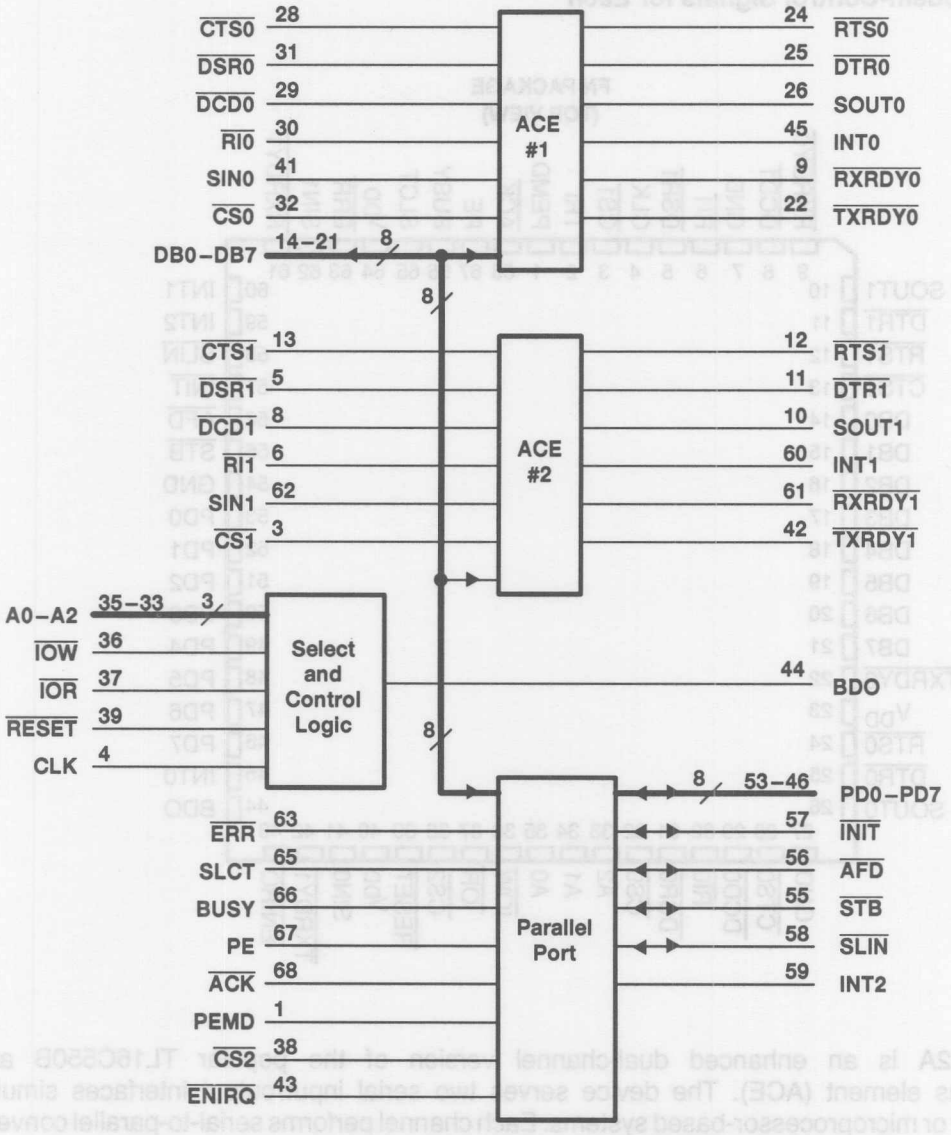
The TL16C552A is an enhanced dual-channel version of the popular TL16C550B asynchronous communications element (ACE). The device serves two serial input/output interfaces simultaneously in microcomputer or microprocessor-based systems. Each channel performs serial-to-parallel conversion on data characters received from peripheral devices or modems and parallel-to-serial conversion on data characters transmitted by the CPU. The complete status of each channel of the dual ACE can be read at any time during functional operation by the CPU. The information obtained includes the type and condition of the transfer operations being performed and the error conditions.

description (continued)

In addition to its dual-communications interface capabilities, the TL16C552A provides the user with a bidirectional parallel data port that fully supports the parallel Centronics-type printer. The parallel port and the two serial ports provide IBM PC/AT-compatible computers with a single device to serve the three system ports. A programmable baud-rate generator is included that can divide the timing-reference clock input by a divisor between 1 and ($2^{16} - 1$).

The TL16C552A is available in a 68-pin plastic leaded chip-carrier (FN) package.

functional block diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{ACK}$	68	I	Line-printer acknowledge. $\overline{ACK}$ goes low to indicate a successful data transfer has taken place. $\overline{ACK}$ generates a printer-port interrupt during its positive transition.
$\overline{AFD}$	56	I/O	Line-printer autofeed. This open-drain line provides the line printer with an active-low signal when continuous form paper is to be autofed to the printer. $\overline{AFD}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
A0, A1, A2	35, 34, 33	I	Address. The address lines A0–A2 select the internal registers during CPU bus operations. See Table 1 for the decode of the serial channels and Table 11 for the decode of the parallel line-printer port.
BDO	44	O	Bus buffer. This active-high output is asserted when either serial channel or the parallel port is read. BDO is used to control the system bus driver (74LS245).
BUSY	66	I	Line-printer busy. BUSY is an input line from the line printer that goes high when the line printer is not ready to accept data.
CLK	4	I	Clock. CLK is the external clock input to the baud-rate divisor of each ACE.
$\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$	32, 3, 38	I	Chip select. Each input acts as an enable for the write and read signals for the serial channels 1 ($\overline{CS0}$) and 2 ($\overline{CS1}$). $\overline{CS2}$ enables the signals to the line-printer port.
$\overline{CTS0}$, $\overline{CTS1}$	28, 13	I	Clear to send. The logical state of each $\overline{CTS}$ terminal is reflected in the CTS bit of the modem-status register (MSR) (CTS is bit 4 of the MSR, written MSR4) of each ACE. A change of state in either $\overline{CTS}$ terminal since the previous reading of the associated MSR causes the setting of ΔCTS (MSR0) of each modem-status register.
DB0-DB7	14-21	I/O	Data bits DB0–DB7. The data bus provides eight I/O lines with 3-state outputs for the transfer of data, control, and status information between the TL16C552A and the CPU. These lines are normally in the high-impedance state except during read operations. D0 is the least significant bit (LSB) and is the first serial data bit to be received or transmitted.
$\overline{DCD0}$, $\overline{DCD1}$	29, 8	I	Data-carrier detect. $\overline{DCD}$ is a modem input whose condition can be tested by the CPU by reading MSR7 (DCD) of the modem-status registers. MSR3 (ΔDCD) of the modem-status register indicates whether the $\overline{DCD}$ input has changed since the previous reading of the MSR. $\overline{DCD}$ has no effect on the receiver.
$\overline{DSR0}$, $\overline{DSR1}$	31, 5	I	Data set ready. The logical state of the DSR terminals is reflected in MSR5 of its associated modem-status register. ΔDSR (MSR1) indicates whether the associated DSR terminal has changed state since the previous reading of the MSR.
$\overline{DTR0}$, $\overline{DTR1}$	25, 11	O	Data terminal ready. Each DTR output can be set (low) by writing a logic 1 to MCR0, modem-control register bit 0 of its associated ACE. This signal is cleared (high) by writing a logic 0 to the DTR bit (MCR0) or whenever a reset occurs. When active (low), DTR indicates that its ACE is ready to receive data.
$\overline{ENIRQ}$	43	I	Parallel-port-interrupt source-mode selection. When low, the AT mode of interrupts is enabled. In this mode, the INT2 output is internally connected to the $\overline{ACK}$ input. If the $\overline{ENIRQ}$ output is tied high, the PS-2 mode of interrupt is enabled and the INT2 output is internally tied to the inverse of the $\overline{PRINT}$ bit in the line-printer status register. INT2 is latched high on the rising edge of $\overline{ACK}$. INT2 is held until the status register is read, which then resets the $\overline{PRINT}$ status bit and INT2.
$\overline{ERR}$	63	I	Line-printer error. $\overline{ERR}$ is an input line from the line printer. The line printer reports an error by holding $\overline{ERR}$ low during the error condition.
GND	7, 27, 54		Ground (0 V). All terminals must be tied to GND for proper operation.
$\overline{INIT}$	57	I/O	Line-printer initialize. This open-drain line provides the line printer with an active-low signal that allows the line-printer-initialization routine to be started. $\overline{INIT}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
INT0, INT1	45, 60	O	External serial-channel interrupt. Each serial-channel-interrupt 3-state output (enabled by bit 3 of the MCR) goes active (high) when one of the following interrupts has an active (high) condition and is enabled by the interrupt-enable register of its associated channel: receiver error flag, received data available, transmitter holding-register empty, and modem status. The interrupt is reset low on appropriate service. Upon reset, the interrupt output is in the high-impedance state.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
INT2	59	O	Printer-port interrupt. INT2 is an active-high, 3-state output generated by the positive transition of $\overline{ACK}$. INT2 is enabled by bit 4 of the write-control register. Upon reset, INT2 is in the high-impedance state. Its mode is also controlled by $\overline{ENIRQ}$.
$\overline{IOR}$	37	I	Input/output read strobe. $\overline{IOR}$ is an active-low input that enables the selected channel to output data to the data bus (DB0–DB7). The data output depends on the register selected by the address inputs A0, A1, A2, and chip select. Chip select 0 ($\overline{CS0}$) selects ACE #1, chip select 1 ($\overline{CS1}$) selects ACE #2, and chip select 2 ($\overline{CS2}$) selects the line-printer port.
$\overline{IOW}$	36	I	Input/output write strobe. $\overline{IOW}$ is an active-low input causing data from the data bus to be input to either ACE or to the parallel port. The destination depends on the register selected by the address inputs A0, A1, A2, and chip selects $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$.
PD0–PD7	53–46	I/O	Parallel data bits (0–7). PD0–PD7 provide a byte-wide input or output port to the system.
PE	67	I	Line-printer paper empty. PE is an input line from the line printer that goes high when the printer runs out of paper.
PEMD	1	I	Printer-enhancement-mode. When low, PEMD enables the write data register to the PD0–PD7 lines. A high on this signal allows direction control of the PD0–PD7 port by the DIR bit in the control register. PEMD is usually tied low for the printer operation.
$\overline{RESET}$	39	I	Reset. When low, $\overline{RESET}$ forces the TL16C552A into an idle mode in which all serial data activities are suspended. The modem-control register (MCR) along with its associated outputs are cleared. The line-status register (LSR) is cleared except for the THRE and TEMT bits, which are set. All functions of the device remain in an idle state until programmed to resume serial data activities. $\overline{RESET}$ has a hysteresis level of typically 400 mV.
$\overline{RTS0}$, $\overline{RTS1}$	24, 12	O	Request to send. The $\overline{RTS}$ outputs are set low by writing a logic 1 to MCR1 bit 1 of its UARTs modem-control register. Both $\overline{RTS}$ terminals are reset high by $\overline{RESET}$. A low on $\overline{RTS}$ indicates that its ACE has data ready to transmit. In half-duplex operations, $\overline{RTS}$ is used to control the direction of the line.
$\overline{RXRDY0}$, $\overline{RXRDY1}$	9, 61	O	Receiver ready. Receiver DMA signaling is also available through this output. One of two types of DMA signaling can be selected via FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. For signal transfer DMA (a transfer is made between CPU bus cycles), mode 0 is used. Multiple transfers that are made continuously until the RCVR FIFO has been emptied are supported by mode 1. Mode 0. $\overline{RXRDY}$ is active (low) when in the FIFO mode (FCR0 = 1, FCR3 = 0) or when in the TL16C450 mode (FCR0 = 0) and the RCVR FIFO or RCVR holding register contain at least one character. When there are no more characters in the FIFO or holding register, $\overline{RXRDY}$ goes inactive (high). Mode 1. $\overline{RXRDY}$ goes active (low) in the FIFO mode (FCR0 = 1) when FCR3 = 1 and the time-out or trigger levels have been reached. $\overline{RXRDY}$ goes inactive (high) when the FIFO or holding register is empty.
$\overline{RI0}$, $\overline{RI1}$	30, 6	I	Ring indicator. The $\overline{RI}$ signal is a modem-control input whose condition is tested by reading MSR6 (RI) of each ACE. The modem-status-register output TERI (MSR2) indicates whether $\overline{RI}$ has changed from high to low since the previous reading of the MSR.
SIN0, SIN1	41, 62	I	Serial data. SIN0 and SIN1 move information from the communication line or modem to the TL16C552A receiver circuits. A mark (1) is high and a space (0) is low. Data on serial-data inputs is disabled when operating in the loop mode.
SLCT	65	I	Line-printer select. SLCT is an input line from the line printer that goes high when the line printer is selected.
$\overline{SLIN}$	58	I/O	Line-printer select. This open-drain I/O selects the printer when active (low). $\overline{SLIN}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.
SOUT0, SOUT1	26, 10	O	Serial-data outputs. These lines are the serial-data outputs from the ACE's transmitter circuitry. A mark is a logic 1 (high) and a space is a logic 0 (low). Each SOUT is held in the mark condition when the transmitter is disabled, $\overline{RESET}$ is true (low), the transmitter register is empty, or when in the loop mode.
$\overline{STB}$	55	I/O	Line-printer strobe. This open-drain line provides communication between the TL16C552A and the line printer. When $\overline{STB}$ is active (low), it provides the line printer with a signal to latch the data currently on the parallel port. $\overline{STB}$ has an internal pullup resistor to V_{DD} of approximately 10 kΩ.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TRI	2	I	3-state output control input. TRI is used to control the 3-state control of all I/O and output terminals. When TRI is asserted, all I/O and outputs are in the high-impedance state allowing board-level testers to drive the outputs without overdriving internal buffers. This CMOS input is level sensitive and is pulled down with an internal resistor that is approximately 5 kΩ.
$\overline{\text{TXRDY0}}$ $\overline{\text{TXRDY1}}$	22 42	O	Transmitter ready. Two types of DMA signaling are available. Either can be selected via FCR3 when operating in the FIFO mode. Only DMA mode 0 is allowed when operating in the TL16C450 mode. Single-transfer DMA (a transfer is made between CPU bus cycles) is supported by mode 0. Multiplication transfers that are made continuously until the XMIT FIFO has been filled are supported by mode 1. Mode 0. When in the FIFO mode (FCR0 = 1, FCR3 = 0) or in the TL16C450 mode (FCR0 = 0) and there are no characters in the XMIT holding register or XMIT FIFO, $\overline{\text{TXRDY}}$ is active (low). Once $\overline{\text{TXRDY}}$ is activated (low), it goes inactive after the first character is loaded into the holding register of the XMIT FIFO. Mode 1. $\overline{\text{TXRDY}}$ goes active (low) if in the FIFO mode (FCR0 = 1) when FCR3 = 1 and there are no characters in the XMIT FIFO. When the XMIT FIFO is completely full, $\overline{\text{TXRDY}}$ goes inactive (high).
V_{DD}	23, 40, 64		Power supply. The V_{DD} requirement is 5 V ±5%.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) ..... −0.5 V to V_{DD} + 0.3 V
Input voltage range, V_I ..... −0.5 V to 7 V
Output voltage range, V_O ..... −0.5 V to V_{DD} + 0.3 V
Continuous total power dissipation at (or below) 70°C ..... 500 mW
Operating free-air temperature range ..... −10°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage levels are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.75	5	5.25	V
Clock high-level input voltage, $V_{IH(CLK)}$	2		V_{DD}	V
Clock low-level input voltage, $V_{IL(CLK)}$	−0.5		0.8	V
High-level input voltage, V_{IH}	2		V_{DD}	V
Low-level input voltage, V_{IL}	−0.5		0.8	V
Clock frequency, f_{clock}			16	MHz
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA for DB0–DB7, I_{OH} = −2 mA for PD0–PD7, I_{OH} = −0.4 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OH} = −0.4 mA for all other outputs	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA for DB0–DB7, I_{OL} = 12 mA for PD0–PD7, I_{OL} = 10 mA for $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$, and $\overline{SLIN}$ (see Note 2), I_{OL} = 2 mA for all other outputs		0.4	V
I_I	Input current	V_{DD} = 5.25 V, All other pins are floating		±10	μA
$I_{I(CLK)}$	Clock input current	V_I = 0 to 5.25 V		±10	μA
I_{OZ}	Off-state output current	V_{DD} = 5.25 V, V_O = 0 with chip deselected, or V_O = 5.25 V with chip and write-mode selected		±20	μA
I_{DD}	Supply current	V_{DD} = 5.25 V, No loads on outputs, SIN0, SIN1, $\overline{DSR0}$, $\overline{DSR1}$, $\overline{DCD0}$, $\overline{DCD1}$, $\overline{CTS0}$, $\overline{CTS1}$, $\overline{RI0}$ and $\overline{RI1}$ at 2 V, Other inputs at 0.8 V, Baud-rate generator f_{clock} = 8 MHz, Baud rate = 56 kbps		50	mA

NOTE 2: These four pins contain an internal pullup resistor to V_{DD} of approximately 10 kΩ.

clock timing requirements over recommended ranges of operating free-air temperature and supply voltage

		MIN	MAX	UNIT
t_{w1}	Pulse duration, CLK high (external clock) (see Figure 1)	31		ns
t_{w2}	Pulse duration, CLK low (external clock) (see Figure 1)	31		ns
t_{w3}	Pulse duration, master reset (see Figure 18)	1000		ns

read-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

		MIN	MAX	UNIT
t_{w4}	Pulse duration, $\overline{IOR}$ low	80		ns
t_{su1}	Setup time, $\overline{CSx}$ valid before $\overline{IOR}$ low (see Note 3)	15		ns
t_{su2}	Setup time, A2–A0 valid before $\overline{IOR}$ low (see Note 3)	15		ns
t_{h1}	Hold time, A2–A0 valid after $\overline{IOR}$ high (see Note 3)	20		ns
t_{h2}	Hold time, chip $\overline{CSx}$ after $\overline{IOR}$ high (see Note 3)	20		ns
t_{d1}	Delay time, $t_{su2} + t_{w4} + t_{d2}$ (see Note 4)	175		ns
t_{d2}	Delay time, $\overline{IOR}$ high to $\overline{IOR}$ or $\overline{IOW}$ low	80		ns

NOTES: 3. The internal address strobe is always active.
4. In the FIFO mode, t_{d1} = 425 ns (min) between reads of the receiver FIFO and the status registers (IIR and LSR).

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write-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

		MIN	MAX	UNIT
t_{w5}	Pulse duration, $\overline{IOW}$ low	80		ns
t_{su4}	Setup time, $\overline{CSx}$ valid before $\overline{IOW}$ low (see Note 3)	15		ns
t_{su5}	Setup time, A2–A0 valid before $\overline{IOW}$ low (see Note 3)	15		ns
t_{su6}	Setup time, DB0–DB7 valid before $\overline{IOW}$ high	15		ns
t_{h3}	Hold time, A2–A0 valid after $\overline{IOW}$ high (see Note 3)	20		ns
t_{h4}	Hold time, $\overline{CSx}$ valid after $\overline{IOW}$ high (see Note 3)	20		ns
t_{h5}	Hold time, DB0–DB7 valid after $\overline{IOW}$ high	15		ns
t_{d3}	Delay time, $t_{su5} + t_{w5} + t_{d4}$	175		ns
t_{d4}	Delay time, $\overline{IOW}$ high to $\overline{IOW}$ or $\overline{IOR}$ low	80		ns

NOTE 3: The internal address strobe is always active.

read-cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Note 5 and Figure 4)

PARAMETER		MIN	MAX	UNIT
t_{pd1}	Propagation delay time from $\overline{IOR}$ low to BDO high or from $\overline{IOR}$ high to BDO low		60	ns
t_{en}	Enable time from $\overline{IOR}$ low to DB0–DB7 valid		60	ns
t_{dis}	Disable time from $\overline{IOR}$ high to DB0–DB7 released	0	60	ns

NOTE 5: V_{OL} and V_{OH} (and the external loading) determine the charge and discharge time.

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 6, 7, and 8)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d5}	Delay time, interrupt THRE† low to SOUT low at start		8	24	RCLK cycles
t_{d6}	Delay time, SOUT low at start to interrupt THRE high	See Note 6	8	9	RCLK cycles
t_{d7}	Delay time, $\overline{IOW}$ (WR THR) high to interrupt THRE high	See Note 6	16	32	RCLK cycles
t_{d8}	Delay time, SOUT low at start to $\overline{TXRDY}$ low	C_L = 100 pF		8	RCLK cycles
t_{pd2}	Propagation delay time from $\overline{IOW}$ (WR THR) low to interrupt THRE low	C_L = 100 pF		140	ns
t_{pd4}	Propagation delay time from $\overline{IOR}$ (RD IIR) high to interrupt THRE low	C_L = 100 pF		140	ns
t_{pd5}	Propagation delay time from $\overline{IOW}$ (WR THR) high to $\overline{TXRDY}$ high	C_L = 100 pF		195	ns

† The acronym THRE is for transmitter-holding-register empty.
NOTE 6: If the transmitter interrupt delay is active, this delay is lengthened by one character time minus the last stop bit time.

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figures 9 through 13)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time from stop to INT high	See Note 7		1	RCLK cycle
t_{pd6}	Propagation delay time from RCLK high to sample CLK high			100	ns
t_{pd7}	Propagation delay time from $\overline{IOR}$ (RD RBR/RD LSR) low to reset interrupt low	C_L = 100 pF		150	ns
t_{pd8}	Propagation delay time from $\overline{IOR}$ (RD RBR) low to $\overline{RXRDY}$ high			150	ns

NOTE 7: The receiver data available indication, the overrun error indication, the trigger level interrupts, and the active $\overline{RXRDY}$ indication are delayed three RCLK cycles in the FIFO mode (FCR0 = 1). After the first byte has been received, status indicators (PE, FE, BI) are delayed three RCLK cycles. These indicators are updated immediately for any further bytes received after RDRBR goes active. There are eight RCLK cycle delays for trigger change-level interrupts.

modem-control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Figure 14)

	PARAMETER	MIN	MAX	UNIT
t_{pd9}	Propagation delay time from $\overline{IOW}$ (WR MCR) high to $\overline{RTS}$ ($\overline{DTR}$) low/high		100	ns
t_{pd10}	Propagation delay time from modem input ($\overline{CTS}$, $\overline{DSR}$) low/high to interrupt high		170	ns
t_{pd11}	Propagation delay time from $\overline{IOR}$ (RD MSR) high to interrupt low		140	ns
t_{pd12}	Propagation delay time from $\overline{RI}$ high to interrupt high		170	ns

parallel-port timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Figures 15, 16, and 17)

		MIN	MAX	UNIT
t_{su7}	Setup time, data valid before $\overline{STB}$ low	1		µs
t_{h6}	Hold time, data valid after $\overline{STB}$ high	1		µs
t_{w6}	Pulse duration, $\overline{STB}$ low	1		µs
t_{d10}	Delay time, BUSY high to $\overline{ACK}$ low	Defined by printer		
t_{d11}	Delay time, BUSY low to $\overline{ACK}$ low	Defined by printer		
t_{w7}	Pulse duration, BUSY high	Defined by printer		
t_{w8}	Pulse duration, $\overline{ACK}$ low	Defined by printer		
t_{d12}	Delay time, BUSY high after $\overline{STB}$ high	Defined by printer		
t_{d13}	Delay time, INT2 low after $\overline{ACK}$ low (see Note 8)		22	ns
t_{d14}	Delay time, INT2 high after $\overline{ACK}$ high (see Note 8)		20	ns
t_{d16}	Delay time, INT2 high after $\overline{ACK}$ high (see Note 8)		24	ns
t_{d17}	Delay time, INT2 low after $\overline{IOR}$ high (see Note 8)		25	ns

NOTE 8: t_{d13}–t_{d17} are all measured with a 15-pF load.

PARAMETER MEASUREMENT INFORMATION

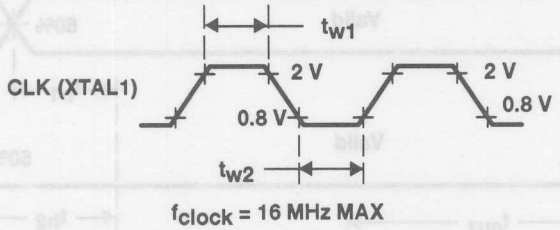
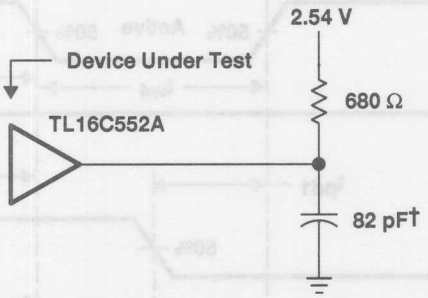


Figure 1. Clock Input (CLK) Voltage Waveform



†Includes scope and jig capacitance

Figure 2. Output Load Circuit

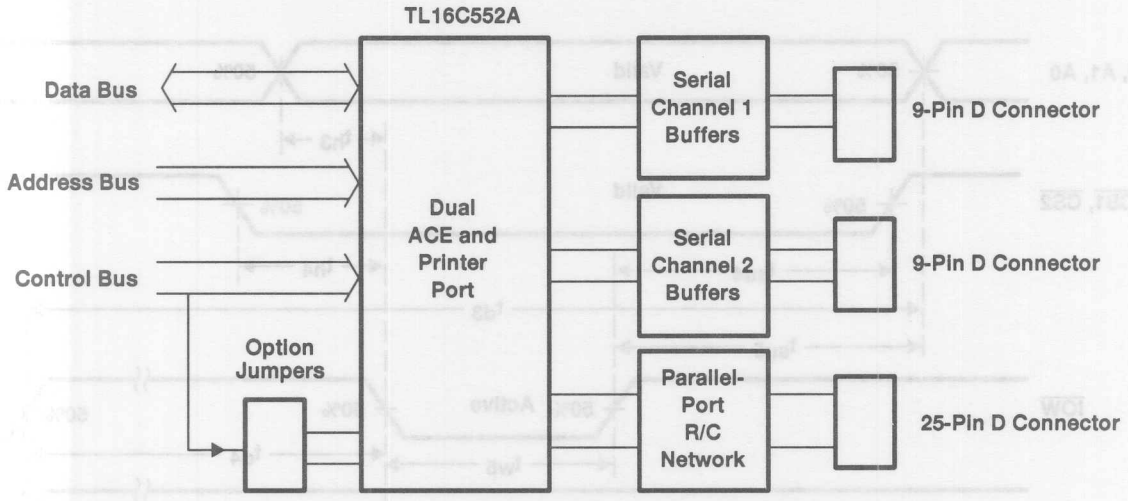


Figure 3. Basic Test Configuration

PARAMETER MEASUREMENT INFORMATION

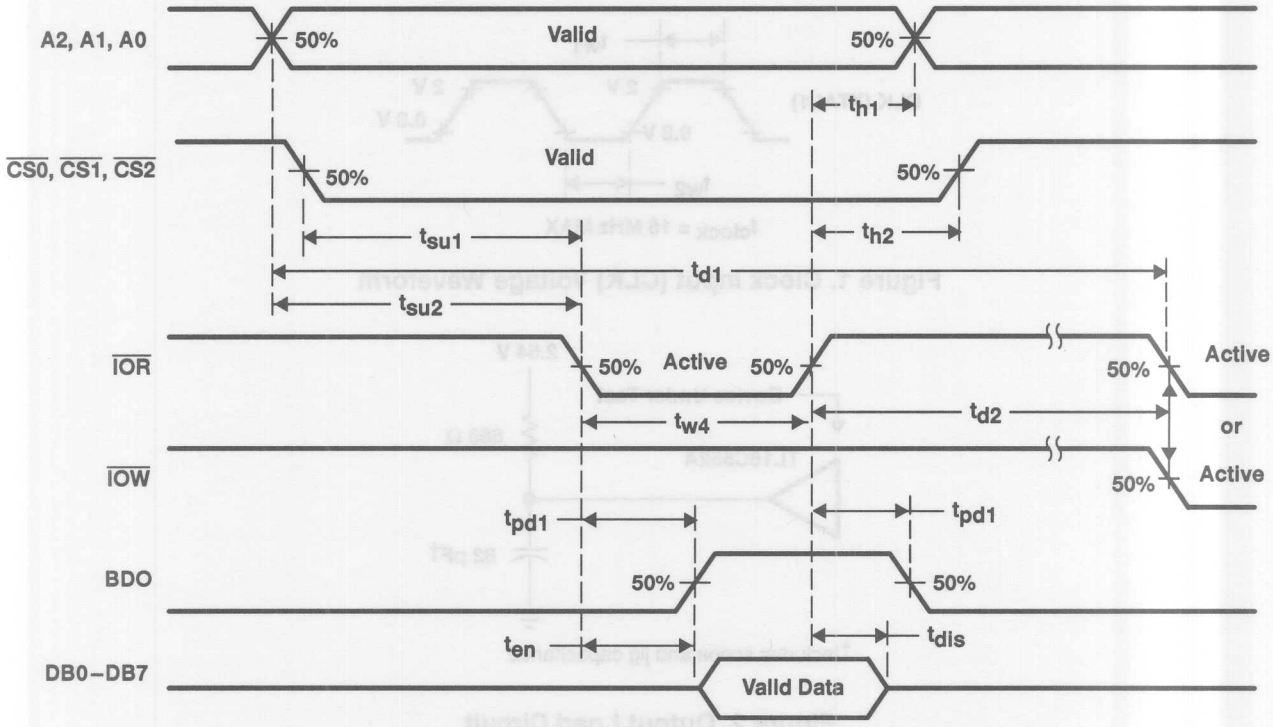


Figure 4. Read-Cycle Timing Waveforms

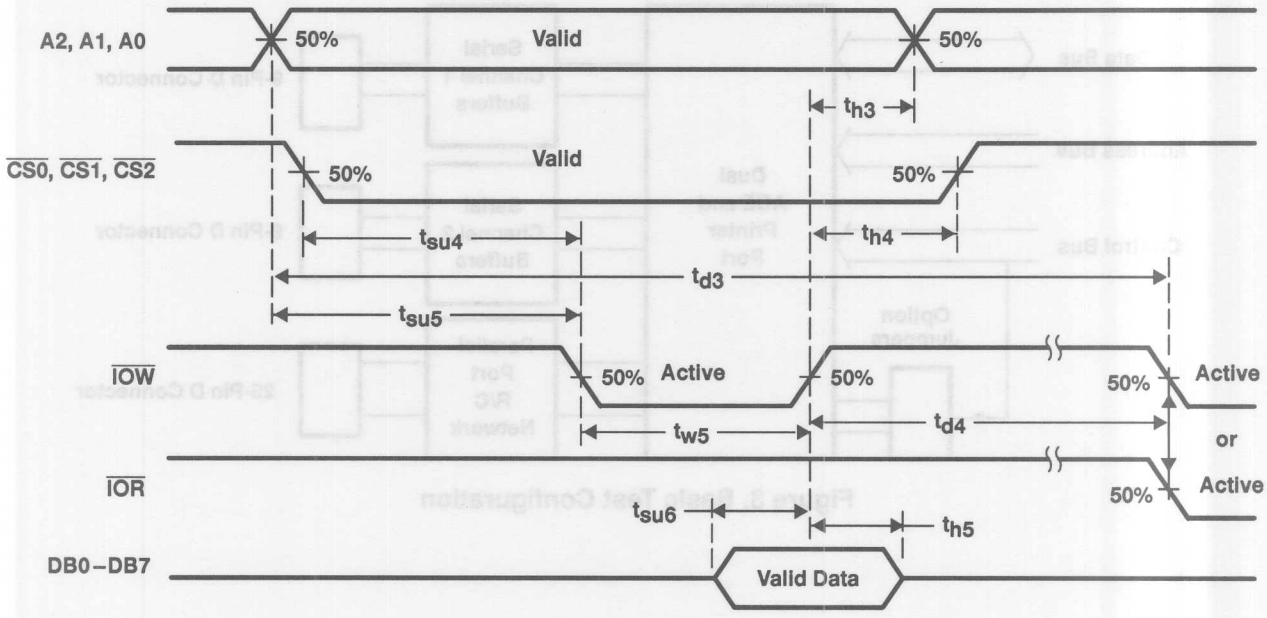


Figure 5. Write-Cycle Timing Waveforms

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PARAMETER MEASUREMENT INFORMATION

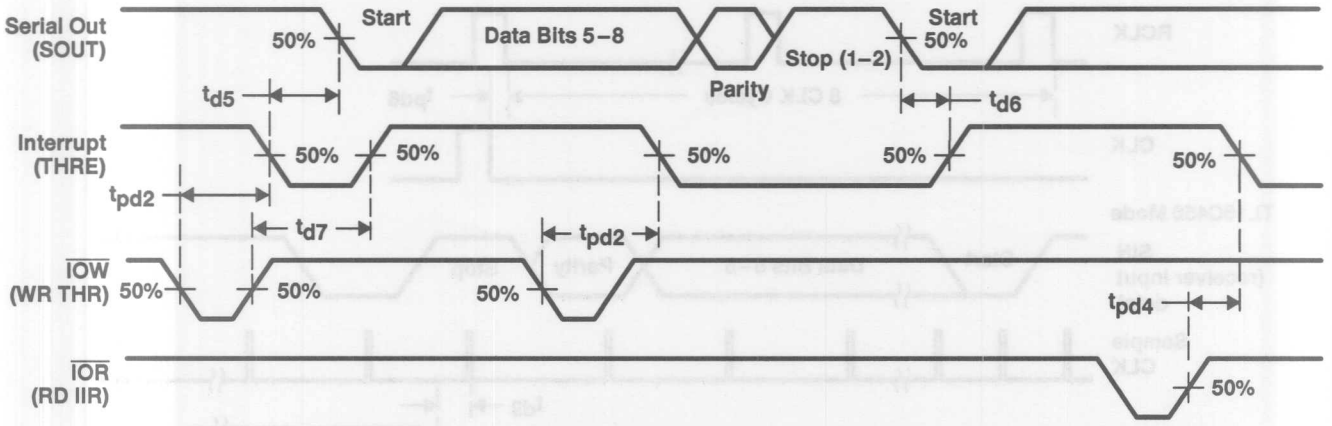

Figure 6. Transmitter Timing Waveforms

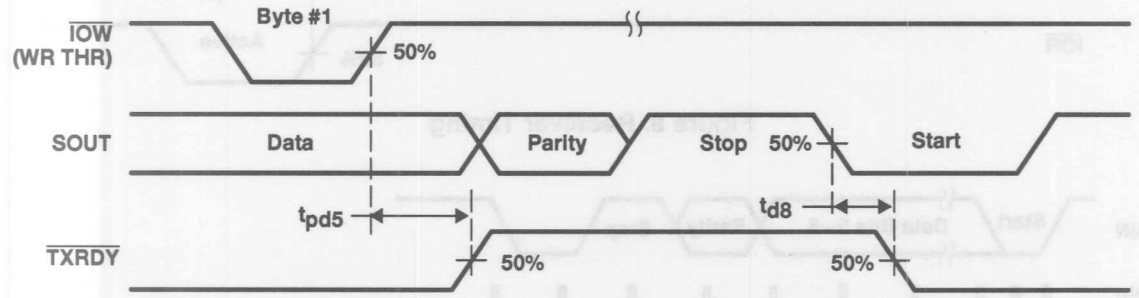

Figure 7. Transmitter Ready-Mode 0 Timing Waveforms

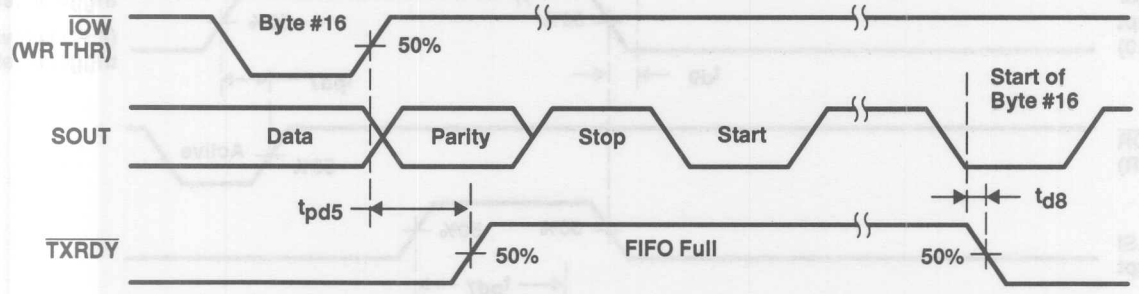

Figure 8. Transmitter Ready-Mode 1 Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

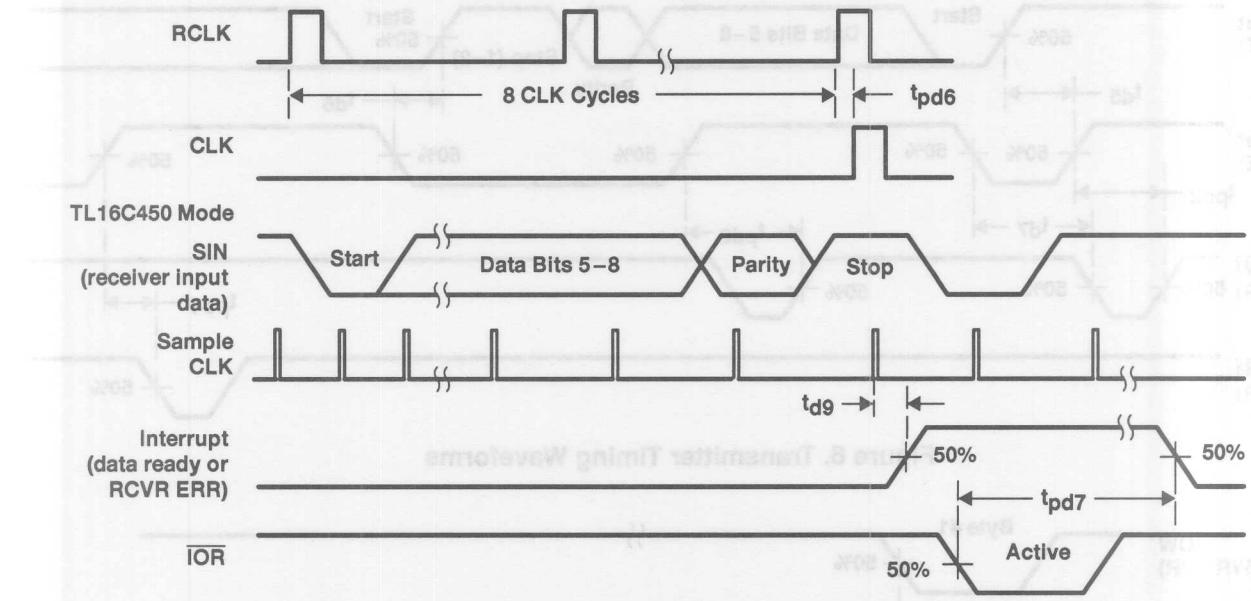

Figure 9. Receiver Timing

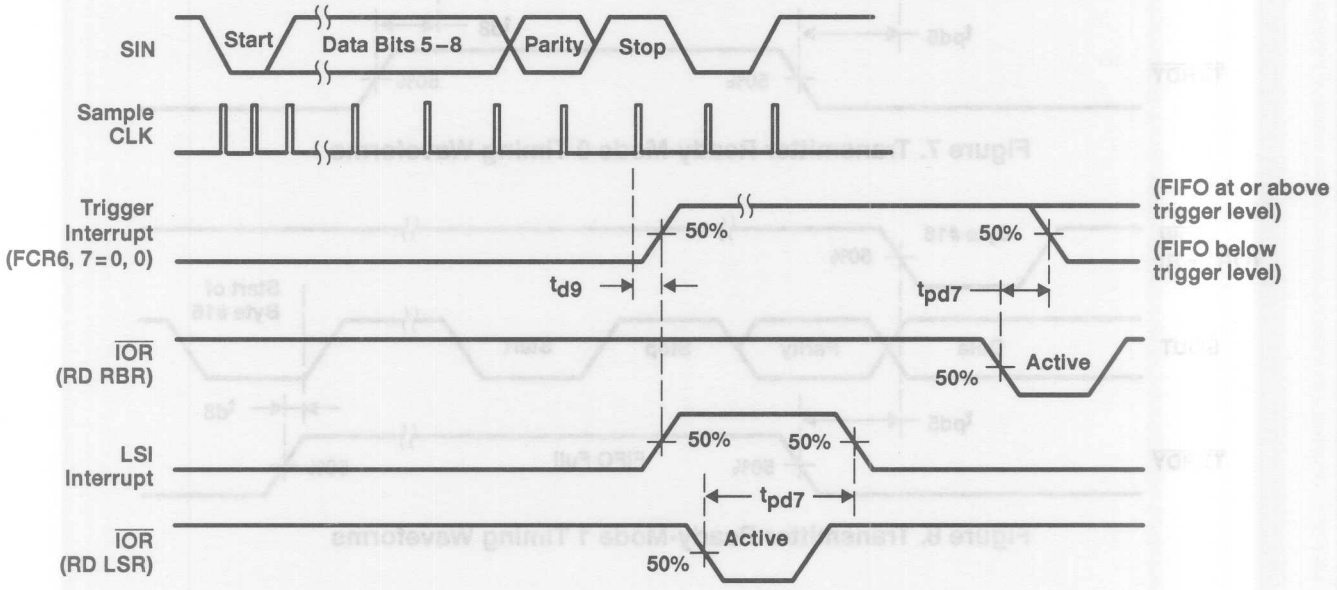

Figure 10. Receiver FIFO First Byte (Sets RDR)

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PARAMETER MEASUREMENT INFORMATION

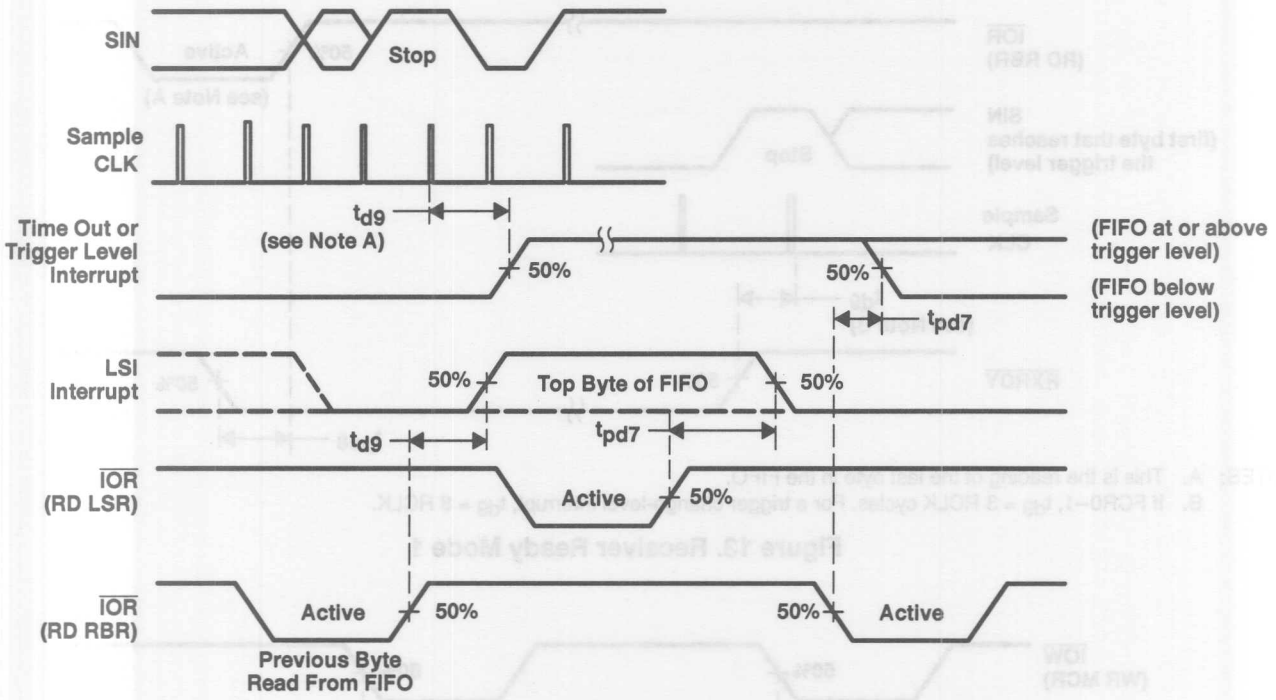


Figure 11. Receiver FIFO After First Byte (After RDR Set)

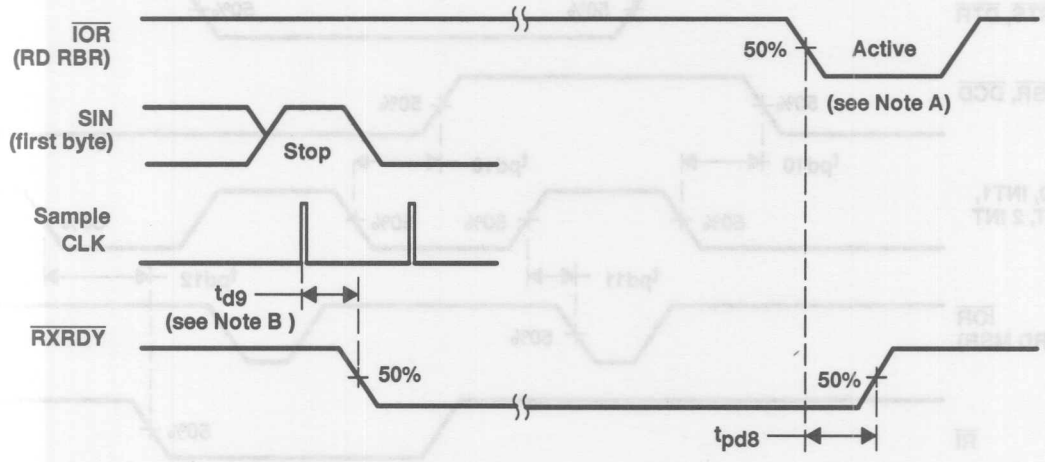
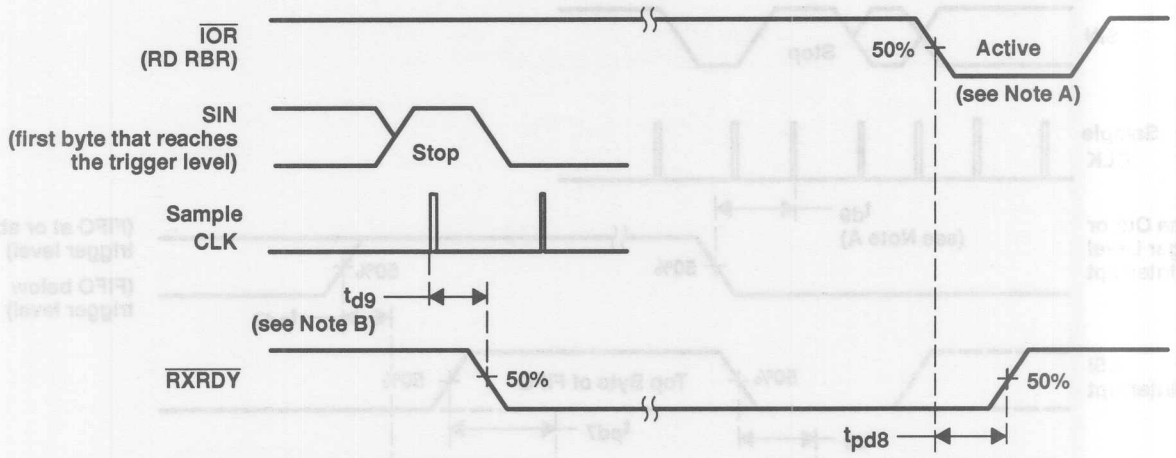


Figure 12. Receiver Ready Mode 0

NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0 = 1, t_{d9} = 3 RCLK cycles. For a time-out interrupt, t_{d9} = 8 RCLK cycles.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. This is the reading of the last byte in the FIFO.
B. If FCR0–1, t_{d9} = 3 RCLK cycles. For a trigger change-level interrupt, t_{d9} = 8 RCLK.

Figure 13. Receiver Ready Mode 1

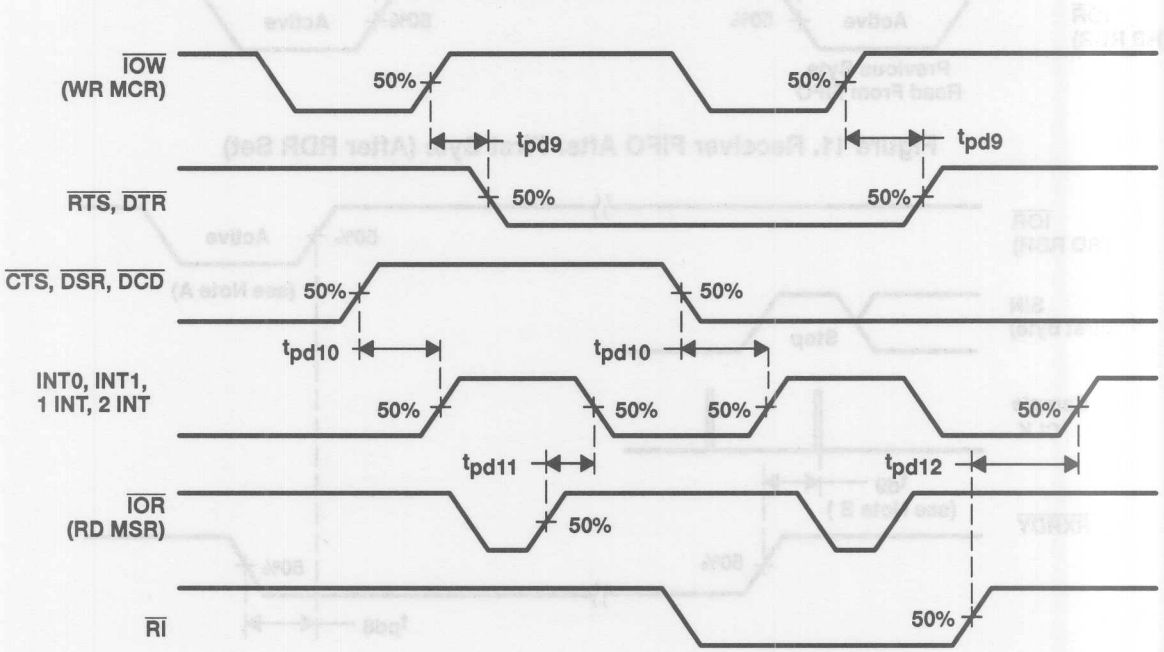


Figure 14. Modem Timing

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PARAMETER MEASUREMENT INFORMATION

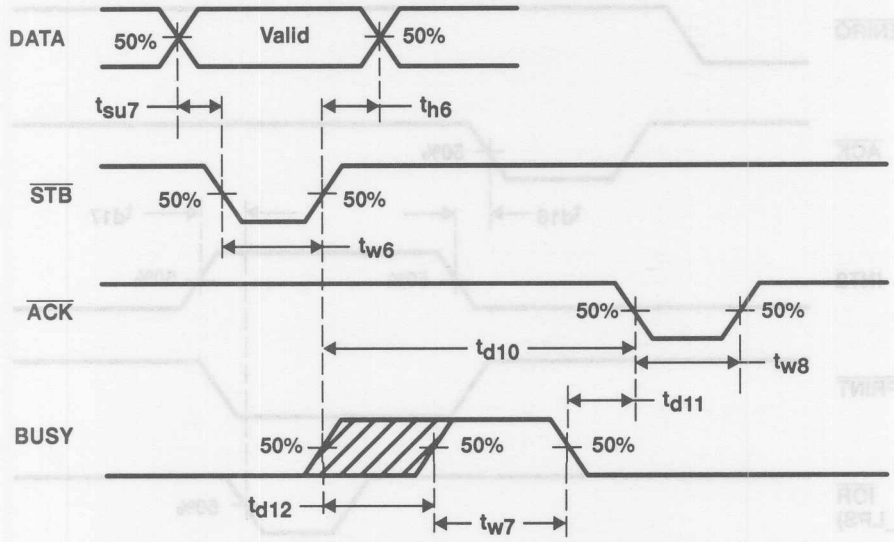
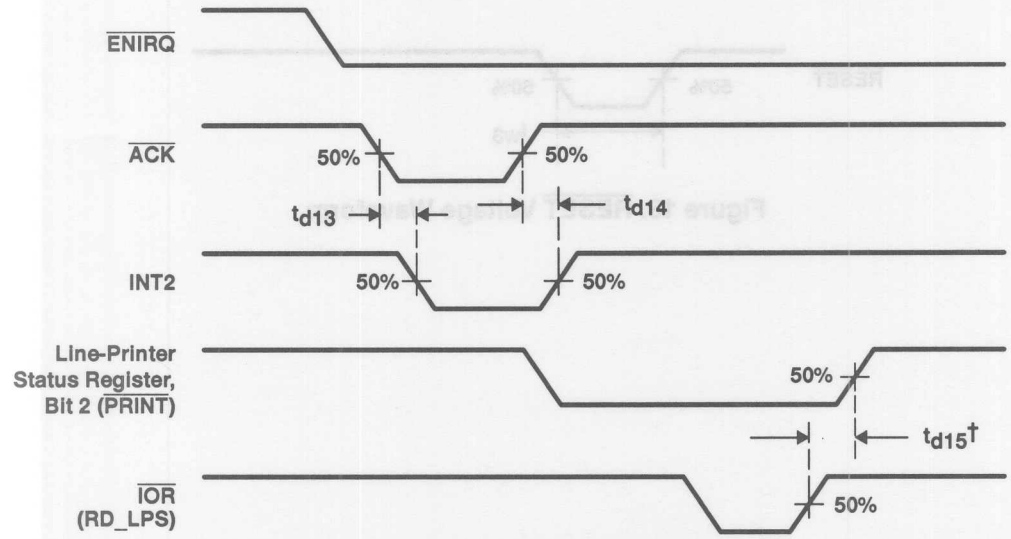


Figure 15. Parallel Port Timing



† A timing value is not provided for t_{d15} in the tables since the line-printer status register, bit 2 ($\overline{PRINT}$) is an internal signal.

Figure 16. Parallel Port AT-Mode Timing (ENIRQ = Low)

PARAMETER MEASUREMENT INFORMATION

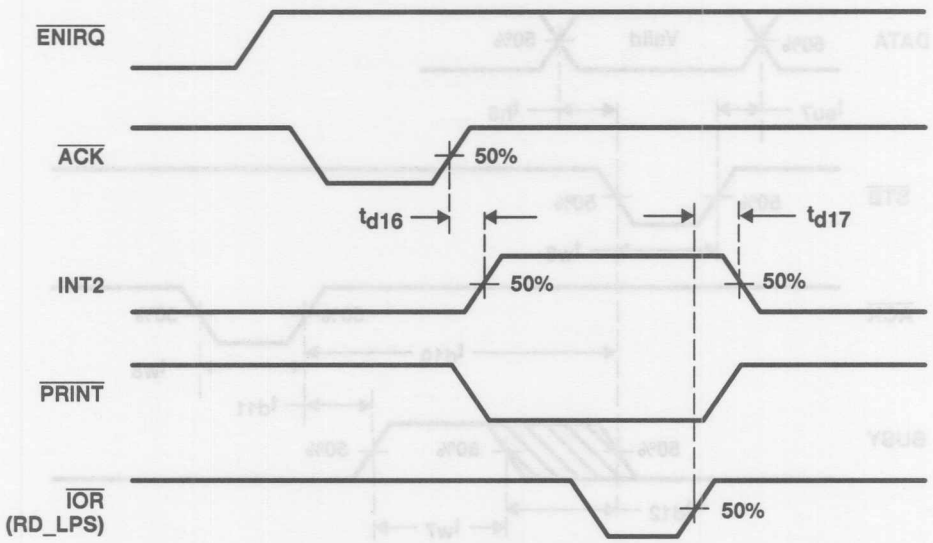


Figure 17. Parallel Port PS/2 Mode Timing (ENIRQ = High)

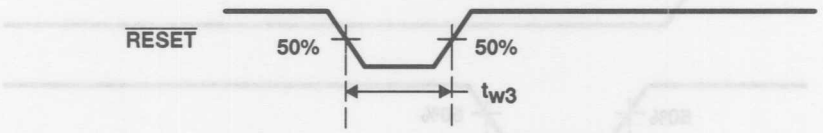


Figure 18. RESET Voltage Waveform

PRINCIPLES OF OPERATION

Three types of information are stored in the internal registers used in the ACE: control, status, and data. Mnemonic abbreviations for the registers are shown in the table below.

CONTROL	MNEMONIC	STATUS	MNEMONIC	DATA	MNEMONIC
Line-control register	LCR	Line-status register	LSR	Receiver-buffer register	RBR
FIFO-control register	FCR	Modem-status register	MSR	Transmitter-holding register	THR
Modem-control register	MCR				
Divisor-latch LSB	DLL				
Divisor-latch MSB	DLM				
Interrupt-enable register	IER				

The address, read, and write inputs are used with the divisor latch access bit (DLAB) in the line-control register (bit 7) to select the register to be written or read (see Table 1). Individual bits within the registers are referred to by the register mnemonic and the bit number in parenthesis. As an example, LCR7 refers to line-control register bit 7.

The transmitter buffer register and receiver buffer register are data registers that hold from five to eight bits of data. If less than eight data bits are transmitted, data is right justified to the LSB. Bit 0 of a data word is always the first serial data bit received and transmitted. The ACE data registers are double buffered (TL16C450 mode) or FIFO buffered (FIFO mode) so that read and write operations can be performed when the ACE is performing the parallel-to-serial or serial-to-parallel conversion.

Table 1. Serial-Channel Internal Registers†

DLAB	A2	A1	A0	MNEMONIC	REGISTER
L	L	L	L	RBR	Receiver-buffer register (read only)
L	L	L	L	THR	Transmitter-holding register (write only)
L	L	L	H	IER	Interrupt-enable register
X	L	H	L	IIR	Interrupt-identification register (read only)
X	L	H	L	FCR	FIFO-control register (write only)
X	L	H	H	LCR	Line-control register
X	H	L	L	MCR	Modem-control register
X	H	L	H	LSR	Line-status register
X	H	H	L	MSR	Modem-status register
X	H	H	H	SCR	Scratch pad register
H	L	L	L	DLL	LSB divisor latch
H	L	L	H	DLM	MSB divisor latch

† The serial channel is accessed when either $\overline{CS0}$ or $\overline{CS1}$ is low.
X = irrelevant, L = low level, H = high level

PRINCIPLES OF OPERATION

line-control register

The format of the data character is controlled by the line-control register. The LCR can be read. Its contents are described below and shown in Figure 19.

LCR0 and LCR1 word-length select bits:

The number of bits in each serial character is programmed as shown.

LCR2 stop-bit select bit:

LCR2 specifies the number of stop bits in each transmitted character. The receiver always checks for one stop bit.

LCR3 parity enable bit:

When LCR3 is high, a parity bit between the last data word bit and stop bit is generated and checked.

LCR4 even-parity select bit:

When enabled, a logic one selects even parity.

LCR5 stick-parity bit:

When parity is enabled (LCR3 = 1), LCR5 = 1 causes the transmission and reception of a parity bit to be in the opposite state from the value of LCR4. This forces parity to a known state and allows the receiver to check the parity bit in a known state.

LCR6 break-control bit:

When LCR6 is set to a logic 1, the serial output (SOUT1/SOUT0) is forced to the spacing state (low). The break-control bit acts only on the serial output and does not affect the transmitter logic. If the following sequence is used, no invalid characters are transmitted because of the break:

Step 1: Load a zero byte in response to the transmitter holding-register-empty (THRE) status indication.

Step 2: Set the break in response to the next THRE status indication.

Step 3: Wait for the transmitter to be idle when transmitter empty status signal is set high (TEMT = 1); then clear the break when the normal transmission has to be restored.

LCR7 divisor-latch access bit (DLAB) bit:

Bit 7 must be set high (logic 1) to access the divisor latches DLL and DLM of the baud-rate generator during a read or write operation. LCR7 must be input low (logic 0) to access the receiver buffer register, the transmitter holding register, or the interrupt-enable register.

PRINCIPLES OF OPERATION

line-control register (continued)

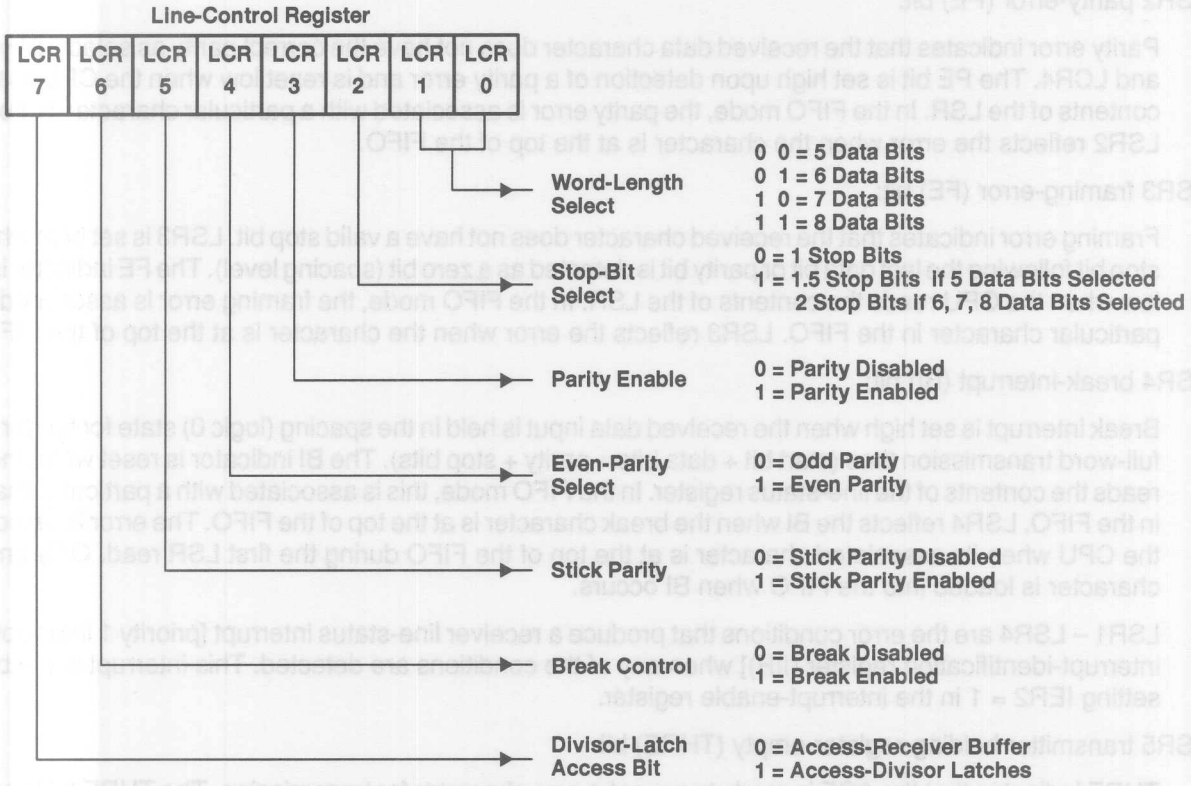


Figure 19. Line-Control Register Contents

line-status register

The line-status register (LSR) is a single register that provides status indications. The line-status register shown in Table 2 is described below:

LSR0 data-ready (DR) bit:

Data ready is set high when an incoming character is received and transferred into the receiver-buffer register or the FIFO. LSR0 is reset low by a CPU read of the data in the receiver-buffer register or the FIFO.

LSR1 overrun-error (OE) bit:

Overrun error indicates that data in the receiver-buffer register is not read by the CPU before the next character is transferred into the receiver buffer register overwriting the previous character. The OE indicator is reset whenever the CPU reads the contents of the line-status register. An overrun error occurs in the FIFO mode after the FIFO is full and the next character is completely received. The overrun error is detected by the CPU on the first LSR read after it happens. The character in the shift register is not transferred to the FIFO, but it is overwritten.

PRINCIPLES OF OPERATION

line-status register (continued)

LSR2 parity-error (PE) bit:

Parity error indicates that the received data character does not have the correct parity as selected by LCR3 and LCR4. The PE bit is set high upon detection of a parity error and is reset low when the CPU reads the contents of the LSR. In the FIFO mode, the parity error is associated with a particular character in the FIFO. LSR2 reflects the error when the character is at the top of the FIFO.

LSR3 framing-error (FE) bit:

Framing error indicates that the received character does not have a valid stop bit. LSR3 is set high when the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset low when the CPU reads the contents of the LSR. In the FIFO mode, the framing error is associated with a particular character in the FIFO. LSR3 reflects the error when the character is at the top of the FIFO.

LSR4 break-interrupt (BI) bit:

Break interrupt is set high when the received data input is held in the spacing (logic 0) state for longer than a full-word transmission time (start bit + data bits + parity + stop bits). The BI indicator is reset when the CPU reads the contents of the line-status register. In the FIFO mode, this is associated with a particular character in the FIFO. LSR4 reflects the BI when the break character is at the top of the FIFO. The error is detected by the CPU when its associated character is at the top of the FIFO during the first LSR read. Only one zero character is loaded into the FIFO when BI occurs.

LSR1 – LSR4 are the error conditions that produce a receiver line-status interrupt [priority 1 interrupt in the interrupt-identification register (IIR)] when any of the conditions are detected. This interrupt is enabled by setting IER2 = 1 in the interrupt-enable register.

LSR5 transmitter holding-register-empty (THRE) bit:

THRE indicates that the ACE is ready to accept a new character for transmission. The THRE bit is set high when a character is transferred from the transmitter-holding register into the transmitter-shift register. LSR5 is reset low by the loading of the transmitter-holding register by the CPU. LSR5 is not reset by a CPU read of the LSR. In the FIFO mode when the XMIT FIFO is empty, this bit is set. It is cleared when one byte is written to the XMIT FIFO. When the THRE interrupt is enabled by IER1, THRE causes a priority 3 interrupt in the IIR. If THRE is the interrupt source indicated in IIR, INTRPT is cleared by a read of the IIR.

LSR6 transmitter empty (TEMT) bit:

TEMT is set high when the transmitter-holding register (THR) and the transmitter-shift register (TSR) are both empty. LSR6 is reset low when a character is loaded into the THR and remains low until the character is transferred out of SOUT. TEMT is not reset low by a CPU read of the LSR. In the FIFO mode, when both the transmitter FIFO and shift register are empty, this bit is set to one.

LSR7 RCVR-FIFO-error bit:

The LSR7 bit is always 0 in the TL16C450 mode. In FIFO mode, it is set when at least one of the following data errors is in the FIFO: parity error, framing error, or break-interrupt indication. It is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.

NOTE: The line-status register may be written. However, this function is intended only for factory test. It should be considered as read only by applications software.

PRINCIPLES OF OPERATION

line-status register (continued)

Table 2. Line-Status Register Bits

LSR BITS	1	0
LSR0 data ready (DR)	Ready	Not ready
LSR1 overrun error (OE)	Error	No error
LSR2 parity error (PE)	Error	No error
LSR3 framing error (FE)	Error	No error
LSR4 break interrupt (BI)	Break	No break
LSR5 transmitter-holding-register empty (THRE)	Empty	Not empty
LSR6 transmitter empty (TEMT)	Empty	Not empty
LSR7 RCVR-FIFO error	Error in FIFO	No error in FIFO

FIFO-control register

This write-only register is at the same location as the IIR. It is used to enable and clear the FIFOs, set the trigger level of the RCVR FIFO, and select the type of DMA signaling.

FCR0 enables both the XMIT and RCVR FIFOs. All bytes in both FIFOs can be cleared by resetting FCR0. Data is cleared automatically from the FIFOs when changing from the FIFO mode to the TL16C450 mode and vice versa. Programming of other FCR bits is enabled by setting FCR0 = 1.

FCR1 = 1 clears all bytes in the RCVR FIFO and resets the counter logic to 0. This does not clear the shift register.

FCR2 = 1 clears all bytes in the XMIT FIFO and resets the counter logic to 0. This does not clear the shift register.

FCR3 = 1 changes the $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ pins from mode 0 to mode 1 if FCR0 = 1.

FCR4 – FCR5: These two bits are reserved for future use.

FCR6 – FCR7: These two bits are used for setting the trigger level for the RCVR FIFO interrupt as follows:

BIT		RCVR-FIFO TRIGGER LEVEL (BYTES)
7	6	
0	0	01
0	1	04
1	0	08
1	1	14

modem-control register

The modem-control register (MCR) controls the interface with the modem or data set as described in Figure 20. MCR can be written and read. The $\overline{\text{RTS}}$ and $\overline{\text{DTR}}$ outputs are directly controlled by their control bits in this register. A high input asserts a low (true) at the output pins. MCR bits 0, 1, 2, 3, and 4 are shown as follows:

MCR0: When MCR0 is set high, the $\overline{\text{DTR}}$ output is forced low. When MCR0 is reset low, the $\overline{\text{DTR}}$ output is forced high. The $\overline{\text{DTR}}$ output of the serial channel may be input into an inverting line driver in order to obtain the proper polarity input at the modem or data set.

PRINCIPLES OF OPERATION

modem-control register (continued)

MCR1: When MCR1 is set high, the $\overline{RTS}$ output is forced low. When MCR1 is reset low, the $\overline{RTS}$ output is forced high. The $\overline{RTS}$ output of the serial channel can be input into an inverting line driver to obtain the proper polarity input at the modem or data set.

MCR2: No effect on operation

MCR3: When MCR3 is set high, the external serial-channel interrupt is enabled.

MCR4: MCR4 provides a local loopback feature for diagnostic testing of the channel. When MCR4 is set high, serial output (SOUT) is set to the marking (logic 1) state and the receiver data input serial input (SIN) is disconnected. The output of the transmitter shift register is looped back into the receiver shift-register input. The four modem-control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected. The modem-control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four modem-control inputs. The modem-control output pins are forced to their inactive (high) state on the TL16C552A. In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the selected serial channel. Interrupt control is fully operational; however, interrupts are generated by controlling the lower four MCR bits internally. Interrupts are not generated by activity on the external pins represented by those four bits.

MCR5 – MCR7 are permanently set to logic 0.

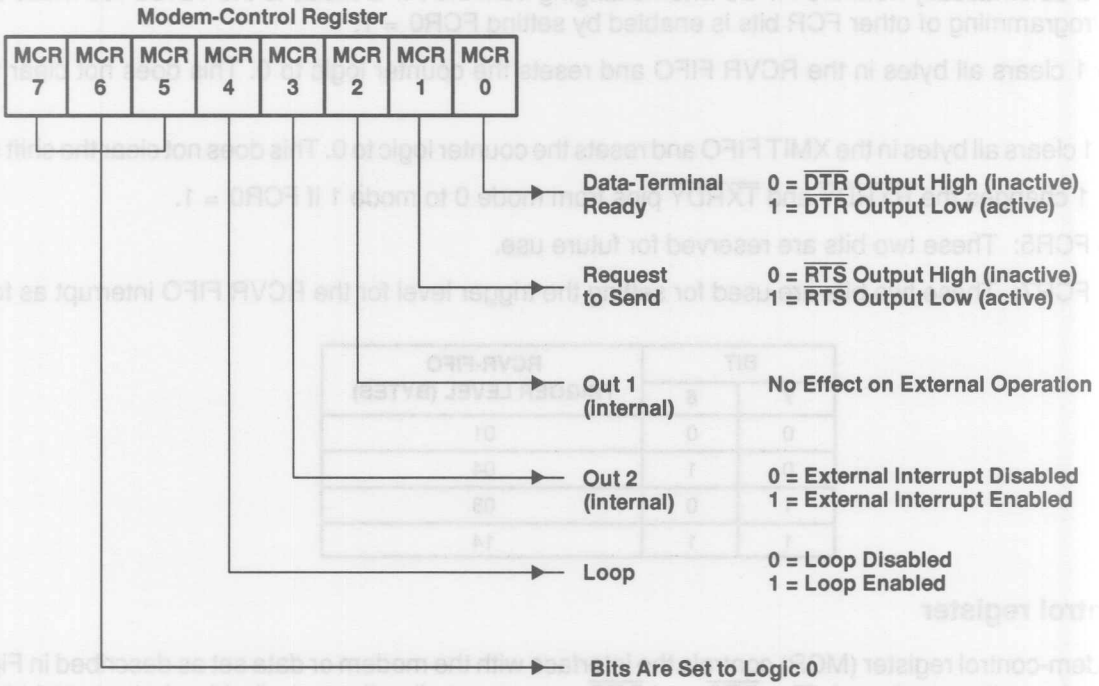


Figure 20. Modem-Control Register Contents

PRINCIPLES OF OPERATION

modem-status register (MSR)

The MSR provides the CPU with status of the modem input lines from the modem or peripheral devices. The MSR allows the CPU to read the serial-channel modem-signal inputs by accessing the data-bus interface of the ACE in addition to the current status of four bits of the MSR that indicate whether the modem inputs have changed since the last reading of the MSR. The delta-status bits are set high when a control input from the modem changes state and resets low when the CPU reads the MSR.

The modem input lines are $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, and $\overline{DCD}$. MSR4 – MSR7 are status indications of these lines. A status bit = 1 indicates the input is low. A status bit = 0 indicates the input is high. If the modem-status interrupt in the interrupt-enable register is enabled (IER3), an interrupt is generated whenever MSR0 – MSR3 is set to a one. The MSR is a priority-4 interrupt. The contents of the modem-status register are described in Table 3.

MSR0, delta clear-to-send (ΔCTS) bit:

ΔCTS displays that the $\overline{CTS}$ input to the serial channel has changed state since it was last read by the CPU.

MSR1, delta data-set-ready (ΔDSR) bit:

ΔDSR indicates that the $\overline{DSR}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR2, trailing-edge of ring-indicator (TERI) bit:

TERI indicates that the $\overline{RI}$ input to the serial channel has changed state from low to high since the last time it was read by the CPU. High-to-low transitions on RI do not activate TERI.

MSR3, delta data-carrier-detect (ΔDCD) bit:

ΔDCD indicates that the $\overline{DCD}$ input to the serial channel has changed state since the last time it was read by the CPU.

MSR4, clear-to-send (CTS) bit:

CTS is the complement of the $\overline{CTS}$ input from the modem indicating to the serial channel that the modem is ready to receive data from the serial channel's transmitter output (SOUT). If the serial channel is in the loop mode (MCR4 = 1), MSR4 reflects the value of RTS in the MCR.

MSR5, data-set-ready (DSR) bit:

DSR is the complement of the $\overline{DSR}$ input from the modem to the serial channel that indicates that the modem is ready to provide received data to the serial-channel receiver circuitry. If the channel is in the loop mode (MCR4 = 1), MSR5 reflects the value of DTR in the MCR.

MSR6, ring-indicator (RI) bit:

RI is the complement of the $\overline{RI}$ input. If the channel is in the loop mode (MCR4 = 1), MSR6 reflects the value of $\overline{OUT1}$ in the MCR.

MSR7, data-carrier-detect (DCD) bit:

Data-carrier detect indicates the status of the data-carrier detect ($\overline{DCD}$) input. If the channel is in the loop mode (MCR4 = 1), MSR7 reflects the value of OUT2 in the MCR.

PRINCIPLES OF OPERATION

modem-status register (continued)

Reading the MSR register clears the delta modem-status indications but has no effect on the other status bits. For LSR and MSR, the setting of status bits is inhibited during status-register read operations. If a status condition is generated during a read $\overline{IOR}$ operation, the status bit is not set until the trailing edge of the read. If a status bit is set during a read operation and the same status condition occurs, that status bit is cleared at the trailing edge of the read instead of being set again. In the loop-back mode, when modem-status interrupts are enabled, the $\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$ input pins are ignored; however, a modem-status interrupt can still be generated by writing to MCR3–MCR0. Applications software should not write to the modem-status register.

Table 3. Modem-Status Register Bits

MSR BIT	MNEMONIC	DESCRIPTION
MSR0	ΔCTS	Delta clear to send
MSR1	ΔDSR	Delta data-set ready
MSR2	TERI	Trailing-edge of ring indicator
MSR3	ΔDCD	Delta data-carrier detect
MSR4	CTS	Clear to send
MSR5	DSR	Data-set ready
MSR6	RI	Ring indicator
MSR7	DCD	Data-carrier detect

divisor latches

The ACE serial channel contains a programmable baud-rate generator (BRG) that divides the clock (dc to 8 MHz) by any divisor from 1 to $2^{16}-1$ (see also BRG description). The output frequency of the baud generator is 16x the data rate [divisor # = clock ÷ (baud rate x 16)] referred to in this document as RCLK. Two 8-bit divisor-latch registers store the divisor in a 16-bit binary format. These divisor-latch registers must be loaded during initialization. Upon loading either of the divisor latches, a 16-bit baud counter is immediately loaded. This prevents long counts on initial load. The BRG can use any of three different popular frequencies to provide standard baud rates. These frequencies are 1.8432 MHz, 3.072 MHz, and 8 MHz. With these frequencies, standard bit rates from 50 to 512 kbps are available. Tables 5, 6, 7, and 8 illustrate the divisors needed to obtain standard rates using these three frequencies.

scratchpad register

The scratchpad register is an 8-bit read/write register that has no effect on either channel in the ACE. It is intended to be used by the programmer to hold data temporarily.

interrupt-identification register

In order to minimize software overhead during data character transfers, the serial channel prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows:

1. Receiver line status (priority 1)
2. Received-data ready (priority 2) or character time out
3. Transmitter holding-register empty (priority 3)
4. Modem status (priority 4)

PRINCIPLES OF OPERATION

interrupt-identification register (continued)

Information indicating that a prioritized interrupt is pending and the type of interrupt is stored in the interrupt-identification register (IIR). The IIR indicates the highest priority interrupt pending. The contents of the IIR are indicated in Table 4.

Table 4. Contents of the Interrupt-Identification Register

INTERRUPT-IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT-RESET CONTROL
0	0	0	1	–	None	None	–
0	1	1	0	First	Receiver line status	OE, PE, FE, or BI	LSR read
0	1	0	0	Second	Received data available	Receiver data available or trigger level reached	RBR read until FIFO drops below the trigger level
1	1	0	0	Second	Character time-out indication	No characters have been removed from or input to the receiver FIFO during the last four character times and there is at least one character in it during this time.	RBR read
0	0	1	0	Third	THRE	THRE	IIR read if THRE is the interrupt source or THR write
0	0	0	0	Fourth	Modem status	$\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$, or $\overline{DCD}$	MSR read

IIR0 can be used to indicate whether an interrupt is pending. When IIR0 is low, an interrupt is pending.

IIR1 and IIR2 are used to identify the highest priority interrupt pending as indicated in Table 4.

IIR3: This bit is always logic 0 when in the TL16C450 mode. This bit is set along with bit 2 when in the FIFO mode and a trigger change-level interrupt is pending.

IIR4 – IIR5: These two bits are always set to logic 0.

IIR6 – IIR7: FCR0 = 1 sets these two bits.

interrupt-enable register

The interrupt-enable register (IER) is used to independently enable the four serial-channel interrupt sources that activate the interrupt (INT0 or INT1) output. All interrupts are disabled by resetting IER0 – IER3 of the interrupt-enable register. Interrupts are enabled by setting the appropriate bits of the IER high. Disabling the interrupt system inhibits the interrupt-identification register and the active (high) interrupt output. All other system functions operate in their normal manner, including the setting of the line-status and modem-status registers. The contents of the interrupt-enable register shown in Table 9 are described below:

IER0. When set to one, IER0 enables the received-data-available interrupt and the time-out interrupts in the FIFO mode.

IER1. When set to one, IER1 enables the transmitter holding-register-empty interrupt.

IER2. When set to one, IER2 enables the receiver line-status interrupt.

IER3. When set to one, IER3 enables the modem-status interrupt.

IER4 – IER7. These four bits of the IER are logic 0.

PRINCIPLES OF OPERATION

receiver

Serial asynchronous data is input into SIN. The ACE continually searches for a high-to-low transition from the idle state. When the transition is detected, a counter is reset and counts the 16× clock to 7 1/2, which is the center of the start bit. The start bit is valid if SIN is still low. Verifying the start bits prevents the receiver from assembling a false data character due to a low-going noise spike on the SIN input.

The line-control register determines the number of data bits in a character (LCR0 and LCR1). If parity is used, LCR3 and the polarity of parity LCR4 is needed. Status for the receiver is provided in the line-status register. When a full character is received, including parity and stop bits, the data-received indication in LSR0 is set high. The CPU reads the receiver-buffer register, which resets LSR0. If the character is not read prior to a new character transfer from the RSR to the RBR, the overrun-error status indication is set in LSR1. If there is a parity error, the parity error is set in LSR2. If a stop bit is not detected, a framing-error indication is set in LSR3.

If the data into SIN is a symmetrical square wave, the center of the data cells occurs within ±3.125% of the actual center, providing an error margin of 46.875%. The start bit can begin as much as one 16× clock cycle prior to being detected.

master reset

After power up, the ACE $\overline{\text{RESET}}$ input should be held low for one microsecond to reset the ACE circuits to an idle mode until initialization. A low on $\overline{\text{RESET}}$ causes the following:

Initializes the transmitter and receiver clock counters

Clears the line-status register (LSR) except for transmitter shift-register empty (TEMT) and transmit holding-register empty (THRE), which are set. The modem-control register (MCR) is also cleared. All of the discrete lines, memory elements, and miscellaneous logic associated with these register bits are also cleared or turned off. The line-control register (LCR), divisor latches, receiver buffer register, and transmitter buffer register are not affected.

Following the removal of the reset condition ($\overline{\text{RESET}}$ high), the ACE remains in the idle mode until programmed. A hardware reset of the ACE sets the THRE and TEMT status bit in the LSR. When interrupts are subsequently enabled, an interrupt occurs due to THRE. A summary of the effect of a reset on the ACE is given in Table 9.

programming

The serial channel of the ACE is programmed by the control registers: LCR, IER, DLL, DLM, MCR, and FCR. These control words define the character length, number of stop bits, parity, baud rate, and modem interface.

While the control registers can be written in any order, the IER should be written last because it controls the interrupt enables. Once the serial channel is programmed and operational, these registers can be updated any time the ACE serial channel is not transmitting or receiving data.

FIFO-interrupt-mode operation

The following RCVR status occurs when the RCVR FIFO and receiver interrupts are enabled:

1. LSR0 is set when a character is transferred from the shift register to the RCVR FIFO. When the FIFO is empty, it is reset.
2. IIR = 06 receiver line-status interrupt has higher priority than the received data-available interrupt IIR = 04.

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FIFO-interrupt-mode operation (continued)

3. Receive data-available interrupt is issued to the CPU when the programmed trigger level is reached by the FIFO. When the FIFO drops below its programmed trigger level, it is cleared.
4. IIR = 04 (receive-data-available indication) also occurs when the FIFO reaches its trigger level. It is cleared when the FIFO drops below the programmed trigger level.

The following RCVR FIFO character time-out status occurs when RCVR FIFO and receiver interrupts are enabled.

1. If the following conditions exist, a FIFO character time-out interrupt occurs:

   Minimum of one character in FIFO

   Last received serial character is longer than four continuous previous character times ago (if two stop bits are programmed, the second one is included in the time delay)

   The last CPU read of the FIFO is more than four continuous character times earlier. At 300 baud and 12-bit characters, the FIFO time-out interrupt causes a latency of 160 ms maximum from received character to interrupt issued.
2. By using the RCLK input for a clock signal, the character times can be calculated. The delay is proportional to the baud rate.
3. The time-out timer is reset after the CPU reads the RCVR FIFO or after a new character is received when there has been no time-out interrupt.
4. A time-out interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

XMIT interrupts occur as follows when the transmitter and XMIT FIFO interrupts are enabled (FCR0 = 1, IER = 1).

1. When the transmitter FIFO is empty, the transmitter holding-register interrupt (IIR = 02) occurs. The interrupt is cleared when the transmitter holding register is written to or the IIR is read. One to sixteen characters can be written to the transmit FIFO when servicing this interrupt.
2. The XMIT-FIFO-empty indications are delayed one character time minus the last stop bit time when the following occurs:

   THRE = 1 and there is not a minimum of two bytes at the same time in XMIT FIFO since the last THRE = 1. The first transmitter interrupt after changing FCR0 is immediate assuming it is enabled.

RCVR-FIFO trigger-level and character time-out interrupts have the same priority as the received-data-available interrupt. The transmitter holding-register-empty interrupt has the same priority as the transmitter FIFO-empty interrupt.

FIFO polled-mode operation

Resetting IER0, IER1, IER2, IER3, or all to zero with FCR0 = 1 puts the ACE into the FIFO polled mode. RCVR and XMITER are controlled separately. Either or both can be in the polled mode.

In the FIFO polled mode, there is no time-out condition indicated or trigger level reached. However, the RCVR and XMIT FIFOs still have the capability of holding characters. The LSR must be read to determine the ACE status.

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Table 5. Baud Rates (1.8432-MHz Clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.690
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.860

Table 6. Baud Rates (3.072-MHz Clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.230
9600	20	–
19200	10	–
38400	5	–

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Table 7. Baud Rates (8-MHz Clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	–
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	–
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.400

Table 8. Baud Rates (16-MHz Clock)

BAUD RATE DESIRED	DIVISOR (N) USED TO GENERATE 16x CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	20000	0.00
75	13334	0.00
110	9090	0.01
134.5	7434	0.01
150	6666	0.01
300	3334	−0.02
600	1666	0.04
1200	834	−0.08
1800	554	0.28
2000	500	0.00
2400	416	0.16
3600	278	−0.08
4800	208	0.16
7200	138	0.64
9600	104	0.16
19200	52	0.16
38400	26	0.16
56000	18	−0.79
128000	8	−2.34
256000	4	−2.34
512000	2	−2.34
1000000	1	0.00

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Table 9. $\overline{\text{RESET}}$

REGISTER/SIGNAL	RESET CONTROL	RESET
Interrupt-enable register	Reset	All bits low (0–3 forced and 4–7 permanent)
Interrupt-identification register	Reset	Bit 0 is high, bits 1, 2, 3, 6, and 7 are low, and bits 4–5 are permanently low.
Line-control register	Reset	All bits low
Modem-control register	Reset	All bits low (5–7 permanent)
FIFO-control register	Reset	All bits low
Line-status register	Reset	All bits are low, except bits 5 and 6 are high.
Modem-status register	Reset	Bits 0–3 low, bits 4–7 input signal
SOUT	Reset	High
Interrupt (RCVR errs)	Read LSR/Reset	Low
Interrupt (RCVR data ready)	Read RBR/Reset	Low
Interrupt (THRE)	Read IIR/Write THR/Reset	Low
Interrupt (modem-status changes)	Read MSR/Reset	Low
$\overline{\text{OUT2}}$	Reset	High
$\overline{\text{RTS}}$	Reset	High
$\overline{\text{DTR}}$	Reset	High
$\overline{\text{OUT1}}$	Reset	High

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Table 10. Serial-Channel Accessible Registers

ADDRESS	REGISTER MNEMONIC	REGISTER BIT NUMBER							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	RBR (read only)	Data Bit 7 (MSB)	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0 (LSB)
0	THR (write only)	Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0
0†	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1†	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1	IER	0	0	0	0	(EDSSI) Enable-modem-status interrupt	(ERLSI) Enable-receiver-line-status interrupt	(ETBEI) Enable-transmitter-holding-register-empty interrupt	(ERBFI) Enable-received-data-available interrupt
2	FCR (write only)	RCVR Trigger (MSB)	RCVR Trigger (LSB)	Reserved	Reserved	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO Enable
2	IIR (read only)	FIFOs Enabled‡	FIFOs Enabled‡	0	0	Interrupt ID Bit 3‡	Interrupt ID Bit 2	Interrupt ID Bit 1	0 If interrupt pending
3	LCR	(DLAB) Divisor-latch-access bit	Set break	Stick parity	(EPS) Even-parity select	(PEN) Parity enable	(STB) Number of stop bits	(WLSB1) Word-length select bit 1	(WLSB0) Word-length select bit 0
4	MCR	0	0	0	Loop	OUT2 Enable external interrupt (INT0 or INT1)	OUT1 (an unused internal signal)	(RTS) Request to send	(DTR) Data-terminal ready
5	LSR	Error in RCVR FIFO‡	(TEMT) Transmitter empty	(THRE) Transmitter holding-register empty	(BI) Break interrupt	(FE) Framing error	(PE) Parity error	(OE) Overrun error	(DR) Data ready
6	MSR	(DCD) Data-carrier detect	(RI) Ring indicator	(DSR) Data-set ready	(CTS) Clear to send	(ΔDCD) Delta-data-carrier detect	(TERI) Trailing-edge ring indicator	(ΔDSR) Delta data-set ready	(ΔCTS) Delta clear to send
7	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

† DLAB = 1
‡ These bits are always 0 when FIFOs are disabled.

parallel-port registers

The TL16C552A parallel port can be used to interface the device to a Centronics-style printer. When chip select 2 ($\overline{CS2}$) is low, the parallel port is selected. Table 11 shows the registers associated with this parallel port. The read or write function of the register is controlled by the state of the read ($\overline{IOR}$) and write ($\overline{IOW}$) pins as shown. The read-data register allows the microprocessor to read the information on the parallel bus.

The read-status register allows the microprocessor to read the status of the printer in the six most significant bits. The status bits are printer busy $\overline{BSY}$, acknowledge ($\overline{ACK}$) (a handshake function), paper empty (PE), printer selected ($\overline{SLCT}$), error ($\overline{ERR}$) and printer interrupt ($\overline{PRINT}$). The read-control register allows the state of the control lines to be read. The write-control register sets the state of the control lines. They are direction (DIR), interrupt enable (INT2 EN), select in ($\overline{SLIN}$), initialize the printer ($\overline{INIT}$), autofeed the paper ($\overline{AFD}$), and strobe ($\overline{STB}$), which informs the printer of the presence of a valid byte on the parallel bus. The write-data register allows the microprocessor to write a byte to the parallel bus. The parallel port is completely compatible with the parallel-port implementation used in the IBM serial parallel adaptor.

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Table 11. Parallel-Port Registers

REGISTER	REGISTER BITS							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Read data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Read status	$\overline{BSY}$	$\overline{ACK}$	PE	SLCT	$\overline{ERR}$	$\overline{PRINT}$	1	1
Read control	0	0	PEMD • DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB
Write data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Write control	0	0	DIR	INT2 EN	SLIN	$\overline{INIT}$	AFD	STB

Table 12. Parallel-Port Register Select

CONTROL PINS					REGISTER SELECTED
$\overline{IOR}$	$\overline{IOW}$	$\overline{CS2}$	A1	A0	
L	H	L	L	L	Read data
L	H	L	L	H	Read status
L	H	L	H	L	Read control
L	H	L	H	H	Invalid
H	L	L	L	L	Write data
H	L	L	L	H	Invalid
H	L	L	H	L	Write control
H	L	L	H	H	Invalid

line-printer port

The line-printer port contains the functionality of the port included in the TL16C452 but offers a hardware-programmable extended mode controlled by the printer-enhancement-mode (PEMD) pin. This enhancement is the addition of a direction-control bit and an interrupt-status bit.

register 0 line-printer data register

The line-printer (LPT) port is either output only or bidirectional depending on the state of the extended-mode pin and data-direction control bits.

Compatibility mode (PEMD pin = L)

Reads to the LPT data register return the last data that was written to the port. Write operations immediately output data to PD0–PD7.

Extended mode (PEMD pin = H)

Read operations return either the data last written to the LPT data register if the direction bit is set to write (low) or the data that is present on PD0–PD7 if the direction is set to read (high). Write operations to the LPT data register latch data into the output register; however, they only drive the LPT port when the direction bit is set to write (low).

The table below summarizes the configuration of the PD port based on the combinations of logic level on the PEMD pin and value of the direction-control bit (DIR).

PEMD	DIR	PD0–PD7 FUNCTION
L	X	PC/AT mode – output
H	0	PS/2 mode – output
H	1	PS/2 mode – input

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register 1 read-line printer-status register

The line-printer-status (LPS) register is a read-only register that contains interrupt and printer status of the LPT connector pins. In the following table (in the default column) are the values of each bit after reset in the case of the printer being disconnected from the port.

BIT	DESCRIPTION	DEFAULT
0	Reserved	1
1	Reserved	1
2	$\overline{\text{PRINT}}$	1
3	$\overline{\text{ERR}}$	†
4	SLCT	†
5	PE	†
6	$\overline{\text{ACK}}$	†
7	$\overline{\text{BSY}}$	†

† Outputs are dependent upon device inputs.

Bits 0 and 1 – Reserved. Read as ones.

Bit 2 – Printer-interrupt ($\overline{\text{PRINT}}$, active low) status bit. Set (low) indicates that the printer has acknowledged the previous transfer with an ACK handshake (if bit 4 of the control register is set to 1). The bit is set to zero on the active to inactive transition of the $\overline{\text{ACK}}$ signal. This bit is set to a one after a read of the status port.

Bit 3 – Error- ($\overline{\text{ERR}}$, active low) status bit corresponds to $\overline{\text{ERR}}$ input.

Bit 4 – Select- (SLCT) status bit corresponds to SLCT input.

Bit 5 – Paper-empty (PE) status bit corresponds to PE input.

Bit 6 – Acknowledge- ($\overline{\text{ACK}}$, active low) status bit corresponds to $\overline{\text{ACK}}$ input.

Bit 7 – Busy- ($\overline{\text{BSY}}$, active low) status bit corresponds to BUSY input (active high).

register 2 line-printer control register

The line-printer control (LPC) register is a read/write port that is used to control the PD0–PD7 direction and drive the printer control lines. Write operations set or reset these bits, while read operations return the state of the last write operation to this register. The bits in this register are defined as follows:

BIT	DESCRIPTION
0	STB
1	AFD
2	$\overline{\text{INIT}}$
3	SLIN
4	INT2 EN
5	DIR
6	Reserved 0
7	Reserved 0

Bit 0 – Printer-strobe (STB) control bit; when 1, the $\overline{\text{STB}}$ signal is asserted on the LPT interface; when 0, the signal is negated.

Bit 1 – Auto-feed (AFD) control bit; when 1, the $\overline{\text{AFD}}$ signal is asserted on the LPT interface; when 0, the signal is negated.

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register 2 line-printer control register (continued)

Bit 2 – Initialize-printer ($\overline{\text{INIT}}$) control bit; when 1, the $\overline{\text{INIT}}$ signal is negated; when 0, the $\overline{\text{INIT}}$ signal is asserted on the LPT interface.

Bit 3 – Select input (SLIN) control bit; when 1, the $\overline{\text{SLIN}}$ signal is asserted on the LPT interface; when 0, the signal is negated.

Bit 4 – Interrupt-request-enable (INT2 EN) control bit; when 1, enables interrupts from the LPT port; when 0, disables interrupts and places INT2 signal in the high-impedance state.

Bit 5 – Direction-(DIR) control bit (only used when PEMD is high); when 1, the output buffers in the LPD port are disabled allowing data driven from external sources to be read from the LPD port. When DIR is 0, the LPD port is in the output mode.

Bits 6 and 7 – Reserved. Read as zeros